REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 3, 5, 7 and 9 have been amended. Claims 14-39 were cancelled without prejudice. No new claims have been added. Therefore, claims 1-13 are presented for examination.

35 U.S.C. § 103 Rejection

Claims 1, 3, 4 and 7-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi et al., U.S. Patent No. 6,109,507 ("Yagi") and Kimura et al., U.S. Patent No. 6,400,034 ("Kimura").

Claim 1, as amended, recites:

> A method comprising:
> applying a no-clean flux to a first surface of a substrate, the first surface of the substrate having attached thereto solder bumps, the solder bumps having a melting temperature, and the no-clean flux substantially comprising ingredients that have a volatilization temperature less than the melting temperature;
> generally aligning the solder bumps with corresponding metal bumps, the metal bumps being attached to a first surface of a chip;
> bringing the solder bumps into contact with the corresponding metal bumps via a thermo-compression bonder;
> heating the solder bumps to a first temperature, the first temperature being equal to or greater than the melting temperature, the solder bumps having a melting point at the first temperature, and the flux having the volatilization temperature at which substantially all of the constituents of the flux volatilize, the volatilization temperature being less than or equal to the first temperature;
> placing the substrate against a first fixture, the first fixture being maintained at a second temperature below the first temperature; and
> placing the chip against a second fixture, the chip having affixed thereto a plurality of metal protrusions.
> (emphasis added)

Applicants respectfully disagree with the Examiner's characterization of Applicant's admitted prior art. The Background section of the Application discloses

"those fluxes that have *volatilization temperature* ***at or above*** *the solder melting point*" (see page 4), which teaches away from and is not the same as "volatilization temperature **less than the** melting temperature" as recited by claim 1. Yagi discloses "forming bumps on pads provided on a board, wherein a plurality of solder bump layer forming cycles are repeatedly implemented." (Abstract) Kimura discloses an object "to provide a high reliable semiconductor device with a chip-size package that has solved the above-mentioned problems." (col. 2, lines 48-51) Yagi and Kimura, neither individually nor when combined, teach or reasonably suggest "the no-clean flux substantially comprising ingredients that have a volatilization temperature less than the melting temperature . . . heating the solder bumps to a first temperature, the first temperature being equal to or greater than the melting temperature, the solder bumps having a melting point at the first temperature, and the flux having the volatilization temperature at which substantially all of the constituents of the flux volatilize, the volatilization temperature being less than or equal to the first temperature . . . placing the substrate against a first fixture, the first fixture being maintained at a second temperature below the first temperature . . . and placing the chip against a second fixture, the chip having affixed thereto a plurality of metal protrusions" as recited by claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection of claim 1 and its dependent claims.

Claims 2 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi and Kimura as applied to claim 1 above, and further in view of Hur et al., U.S. Patent No. 6,013,572 ("Hur").

Claims 3, 4 and 7-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi and further in view of Kimura.

Claim 6 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi and Kimura as applied to claim 1 above, and further in view of Arbib, et al., European Patent No. 0077622 ("Arbib").

Claims 2-13 depend from claim 1 and thus, include all the limitations of claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 2-13.

Conclusion

In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: October 10, 2006

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